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EXAMINER	
KROFCHECK, MICHAEL C	

ART UNIT	PAPER NUMBER
2186	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/759,939	JOHNS, CHARLES RAY	
	Examiner	Art Unit	
	Michael Krofcheck	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☒ Claim(s) *1-11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/759,939 filed on 1/16/2004.

2. Claims 1-13 have been submitted for examination.

3. Claims 1-13 have been examined.

Claim Objections

4. Claims 1-11 objected to because of the following informalities:

   a. Line 10-13 of claim 1 states the cache coherency controller can determine the priority receipt status of a transaction request received from the cache coherency controller (itself). It doesn't make sense for that request to go through a high speed bus since it is internal to the cache coherency controller

   b. The claims not mentioned are objected to because of their dependency.

   Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-11 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. Claim 1 recites the limitation "said master processor" in line 8. There is insufficient antecedent basis for this limitation in the claim.

8. Claim 2 recites the limitation "the step of deploying" in line 6 of the claim. There is insufficient antecedent basis for this limitation in the claim.

9. Claim 3 recites the limitation "said burst operation" and "said snoop replies" in line 1 and lines 9-10 of the claim. There is insufficient antecedent basis for this limitation in the claim.

10. Claim 6 recites the limitation "said snooping said burst operation" in line 1-2 of the claim. There is insufficient antecedent basis for this limitation in the claim.

11. Claim 7 recites the limitations "the total number of indica" and "said agglomerated burst operation" in lines 1-2 of the claim. There is insufficient antecedent basis for this limitation in the claim.

12. Additionally, claim 7 is indefinite and confusing as it is unclear what the applicant is claiming. It appears that the agglomerated burst operation is part of the total number of indicia. The examiner is quite confused by this. Is the agglomerated burst operation made up of the each indicia in the total number of indicia?

13. Claim 8 recites the limitation "said processor support of coherency" in line 1-2 of the claim. There is insufficient antecedent basis for this limitation in the claim.

14. Claim 9 recites the limitation "the broadcast of said burst transfer" in line 1-2 of the claim. There is insufficient antecedent basis for this limitation in the claim.

15. Claim 10 recites the limitation " the step of queuing said cachelines" in line 2-3 of the claim. There is insufficient antecedent basis for this limitation in the claim.

16. All claims not specifically mentioned are rejected because of their dependency.

Claim Rejections - 35 USC § 101

17. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

18. Claim 13 rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claim 13 is directed to a computer program, which is not tangibly embodied. The computer program must be tangibly embodied on a computer readable medium.

Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

21. Claim 1, 6-7 rejected under 35 U.S.C. 103(a) as being unpatentable over Luick et al., US patent 6088769, Suzuki, US patent 5623629, Wicki et al., US patent application publication 2003/0200395, and Sherman, US patent 6877071.

22. With respect to claim 1, Luick teaches of a multiprocessor system (fig. 1), including at least two processors (fig. 1; items 101, 103, 119; column 3, line 65- column 4, line 23), and a cache coherency controller (fig. 1; items 113, 109; column 4, lines 3-10), coupled to address concentration devices (fig. 1; items 105, 115, 117; column 4; lines 2-10; as a memory contains addressed storage locations, it is a concentration of addresses), a method operable in said cache coherency controller for improving coherent data transfers comprising the steps of: initiating a first memory transaction request command from said master processor or said cache coherency controller to a first processor of said multiple processors (fig. 1, 3; column 6, lines 49-63; where the processor (master processor) requests data from the cache controller, which in turn sends the request to the control processor (first processor));

Luick fails to explicitly teach of determining, within said cache coherency controller, priority receipt status of a next memory transaction request from a subsequent processor or the cache coherency controller through high speed busses.

However, Suzuki teaches of determining, within said cache coherency controller, priority receipt status of a next memory transaction request from a subsequent processor or the cache coherency controller through high speed busses (fig. 2; column 1, lines 46-49; column 3, lines 20-24; where the cache controller determines the priority

between the invalidation request (next memory transaction) and the other access requests to the cache memory).

Luick and Suzuki fails to explicitly teach of expanding snoop responses and accumulated snoop responses to provide a coherency action for all cacheline requests utilizing a burst command.

However, Wicki teaches of expanding snoop responses and accumulated snoop responses to provide a coherency action for all cacheline requests utilizing a burst command (fig. 4, 5; paragraph 0042, 0053; where the device provides a writeback in a burst of four rows (cachelines). It is abundantly clear to one of ordinary skill in the art that these writebacks are based on the bursted snoop responses).

Luick, Suzuki, and Wicki fails to explicitly teach of forwarding said transaction requests from said master or said controller to a solitary global serialization device, said serialization device further comprising a multiple cacheline request indicator.

However, Sherman teaches of forwarding said transaction requests from said master or said controller to a solitary global serialization device, said serialization device further comprising a multiple cacheline request indicator (fig. 1, 3b, items 320, 340, 342; column 3, lines 22-29; column 6, lines 53-67; data is provided serially (in bursts) to the data transfer block (serialization device). It is abundantly clear to one of ordinary skill in the art that the provided data can be from the controller or CPU (master). Signals B1-SD and B2-SD indicate the length of the burst (multiple cacheline indicator)).

Luick and Suzuki are analogous arts as they are both in the same field of endeavor, cache coherency. It would have been obvious to one of ordinary skill in the

art having the teachings of Luick and Suzuki at the time of the invention to incorporate determining the priority of cache requests in Suzuki as taught in Luick. Their motivation would have been to ensure that data in the cache memory is not invalidated while it is being used.

The combination of Luick and Suzuki, and Wicki are analogous arts as they are both in the same field of endeavor, cache memories. It would have been obvious to one of ordinary skill in the art having the teachings of Luick, Suzuki, and Wicki at the time of the invention to incorporate the use of bursting snoop operations and writeback operations to the cache in the combination of Luick and Suzuki as taught in Wicki. Their motivation would have been to improve efficiency by using a single burst transfer instead of multiple transfer operations (Wicki, paragraph 0005).

The combination of Luick, Suzuki and Wicki, and Sherman are analogous arts as they are both in the same field of endeavor, bursting memory access. It would have been obvious to one of ordinary skill in the art having the teachings of Luick, Suzuki, Wicki, and Sherman at the time of the invention to include the data transfer blocks, and the address/command scheduler from Sherman into the combination of Luick, Suzuki, and Wicki. Their motivation would have been to decrease the time needed to access memory by simultaneous/parallel writing/reading of the burst operation in the memory.

23. With respect to claim 6, Wicki teaches of wherein said snooping said burst operation comprises at least a bus and at least a cache directly supporting a burst operation (fig. 4, 5; paragraph 0036, 0042).

24. With respect to claim 7, Wicki teaches of wherein the total number of indicia comprising said agglomerated burst operation results in a decrease in coherency indicia traffic (fig. 5; paragraph 0053; where the writeback burst modifies 4 cachelines with the single command, thus reducing traffic over the bus).

25. Claim 2 rejected under 35 U.S.C. 103(a) as being unpatentable over The combination of Luick, Suzuki, Wicki, and Sherman as applied to claim 1 above, and further in view of Galles, US patent 5655102, and Benkual.

26. With respect to claim 2, The combination of Luick, Suzuki, Wicki, and Sherman fails to explicitly teach of the step of determining the precedence of the priority receipt includes the steps of: associating a memory transaction request with a unique identifying tag, said tag forwarded to said serialization device, and wherein the step of deploying a first request command includes the step of: broadcasting the first command and subsequent commands as reflected commands to a plurality of devices.

However, Galles teaches of associating a memory transaction request with a unique identifying tag (column 1, lines 23-27; where each transaction must be tagged so that the requesting node and replying node can keep track of its status. As it is used so the transaction can be kept track of, the tag must uniquely identify the transaction).

Benkual teaches of wherein the step of deploying a first request command includes the step of: broadcasting the first command and subsequent commands as reflected commands to a plurality of devices (abstract; where the systems reflects received command to local caches of the other processors in the system).

The combination of Luick, Suzuki, Wicki, and Sherman, and Galles are analogous arts as they are both in the same field of endeavor, multiprocessor systems. It would have been obvious to one of ordinary skill in the art having the teachings of Luick, Suzuki, Wicki, Sherman, and Galles at the time of the invention to incorporating the tagging of each transaction in the combination of Luick, Suzuki, Wicki, and Sherman as taught in Galles. Their motivation would have been to keep track of the transaction's status (Galles, column 1, lines 23-27). Additionally, as the tag is part of the transaction, when the transaction is sent to the data transfer block in the combination of Luick, Suzuki, Wicki, and Sherman, and Galles, so is the tag.

The combination of Luick, Suzuki, Wicki, Sherman, and Galles, and Benkual are analogous arts as they are both in the same field of endeavor, multiprocessor systems. It would have been obvious to one of ordinary skill in the art having the teachings of Luick, Suzuki, Wicki, Sherman, Galles, and Benkual at the time of the invention to incorporate the reflecting of the received commands to the other processors in the combination of Luick, Suzuki, Wicki, Sherman, and Galles as taught in Benkual. Their motivation would have been so that other processors may keep their caches coherent (Benkual, 0005).

27. Claim 12 rejected under 35 U.S.C. 103(a) as being unpatentable over Benkual et al., US patent application publication 2004/0073623, Wicki, and Palanca et al., US patent 6546462.

28. With respect to claim 12, Benkual teaches of authenticating code in a computer system, a computer program comprising: computer code for determining memory

transaction requests from a master controller or cache coherency controller (paragraph 0010; where the systems receives a command to perform a memory operation from a processor (master controller). This command is received at a bridge coupled to the local caches of the processors. As the command is sent by a processor, it must have been controlled by the code operating on the processor);

computer code for verifying memory transaction requests (fig. 4; paragraph 0041; where the controller includes that ensures that commands directed to the same address are handled in sequence. It is abundantly clear to one of ordinary skill in the art that the circuitry is controlled by a program);

computer code for verifying memory transaction request responses (fig. 4, paragraph 0040; where after all the responses are received, the accumulated response is sent out. It is abundantly clear to one of ordinary skill in the art that there is code monitoring to verify that all the responses have been received);

computer code for agglomerating transaction responses from a plurality of snoop contentions and bus request (fig. 3, 4; paragraph 0034, 0037, 0040; where a second snoop operation is accumulating snoop responses. It is abundantly clear to one of ordinary skill in the art that the snoop operation is running computer code); and

computer code for initiating a single combined burst operation command ().

Benkual fails to explicitly teach of computer code for initiating a single combined burst operation command. However, Wicki teaches of computer code for initiating a single combined burst operation command (fig. 4, 5; paragraph 0053; where writeback

operation is a burst of 4 cachelines. It is abundantly clear to one of ordinary skill in the art that the burst operation is controlled by software).

Benkual and Wicki fails to explicitly teach of a computer program product having a medium with a program embodied on. However, Palanca teaches of a computer program product having a medium with a program embodied on (column 9, lines 1-3).

Benkual and Wicki are analogous arts as they are both in the same field of endeavor, cache coherency. It would have been obvious to one of ordinary skill in the art having the teachings of Benkual and Wicki at the time of the invention to incorporate the use of bursting snoop operations and writeback operations to the cache in Benkual as taught in Wicki. Their motivation would have been to improve efficiency by using a single burst transfer instead of multiple transfer operations (Wicki, paragraph 0005).

The combination of Benkual and Wicki, and Palanca are analogous arts as they are both in the same field of endeavor, cache memories. It would have been obvious to one of ordinary skill in the art having the teachings of Benkual, Wicki, and Palanca at the time of the invention to include the software/firmware controlling the operations in the combination of Benkual and Wicki on a removable medium. Their motivation would have been to provide mobility and allow for upgrades of the control software.

29. Claim 13 rejected under 35 U.S.C. 103(a) as being unpatentable over Mayfield, US patent application publication 2003/0093657, Berg et al., US patent application publication 2003/0131203, Allen et al., US patent application publication 2003/0101297, and Wicki.

30. With respect to claim 13, Mayfield teaches of a computer program for providing improved transfers on a coherent bus in a computer system, the transfer including a computer program comprising: computer code for determining device snoops (paragraph 0002; where each processor generates a snoop response to the snooped commands. As this is completed by the processor, there must be a program telling the processor how to complete it);

computer code for agglomerating a combined response from snoop contentions and bus requests (paragraph 0002; where the system bus switch combines the individual processor snoop responses. It is abundantly clear to one of ordinary skill in the art that the system bus switch contains a program that instructs it to do such);

computer code for broadcasting commands to devices from an agglomerated response (paragraph 0002; where the system bus switch sends the combined snoop responses back to each processor. It is abundantly clear to one of ordinary skill in the art that the system bus switch contains a program that instructs it to do such).

Mayfield fails to explicitly teach of computer code for concentrating addresses of responses from processors and devices. However, Berg teaches of computer code for concentrating addresses of responses from processors and devices (fig. 1, 2; paragraph 0042; where the ACL contains addresses of requests and responses received via the tag and address crossbar, entered by a transaction. It is abundantly clear to one of ordinary skill in the art that the control agent contains a program that enables it to store and address in the ACL).

Berg also teaches of determining a transaction conflict (paragraph 00042).

Mayfield and Berg fails to explicitly teach of computer code for issuing a command to the original initiator of the command for reissuance of the command. However, Allen teaches of computer code for determining a resource conflict and issuing a command to the original initiator of the command for reissuance of the command (fig. 3; paragraph 0021; where the switch responds to the processor of the request and indicates that the request should be retried after a delay if the resources are not available. It is abundantly clear to one of ordinary skill in the art that the switch contains a program that instructs it to do such).

Mayfield, Berg, and Allen fails to specifically teach of burst transfer. However, Wicki teaches of burst transfer (fig. 4, 5; paragraph 0042 0053).

Mayfield and Berg are analogous arts as they are both in the same field of endeavor, memory coherency in multiprocessor systems. It would have been obvious to one of ordinary skill in the art having the teachings of Mayfield and Berg at the time of the invention to include the ACL and the controls for using it of Berg into Mayfield. Their motivation would have been to provide and maintain a list of conflicted transactions (Berg, paragraph 0042).

The combination of Mayfield and Berg, and Allen are analogous arts as they are both in the same field of endeavor, multiprocessor systems. It would have been obvious to one of ordinary skill in the art having the teachings of Mayfield, Berg, and Allen at the time of the invention to enable the switch of the combination of Mayfield and Berg to indicate to the requesting processor that there is an error and it needs to resend

the request after a delay. Their motivation would have been to avoid a live lock condition (Allen paragraph 0003,0004).

The combination of Mayfield, Berg, and Allen and Wicki are analogous arts as they are both in the same field of endeavor, memory coherency. It would have been obvious to one of ordinary skill in the art having the teachings of Mayfield, Berg, Allen and Wicki at the time of the invention to the use of bursting snoop operations in the combination of Mayfield, Berg, and Allen as taught in Wicki. Their motivation would have been to improve efficiency by using a single burst transfer instead of multiple transfer operations (Wicki, paragraph 0005).

Allowable Subject Matter

31. Claim 3-5, 8-11 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

32. The following is a statement of reasons for the indication of allowable subject matter:

c. With respect to claim 3 and its dependent claims (4-5, 8-11), the prior art does not teach of concentrating all addresses of said snoop replies.

Conclusion

33. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

34. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Krofcheck whose telephone number is 571-272-8193. The examiner can normally be reached on Monday - Friday.

35. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

36. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Michael Krofcheck

MATTHEW D. ANDERSON
PRIMARY EXAMINER